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Low-Cost Lattice Matching Si Based Composite Substrates for HgCdTe

by Yuanping Chen

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14. ABSTRACT

A new class of low-cost composite substrate based on ternary alloy $CdSe_xTe_{1-x}$(211)/Si(211) has been developed using molecular beam epitaxy (MBE). Composition of the alloy can be tuned to exactly match the lattice of HgCdTe epilayer to minimize the generation of dislocations at the interface. The growth of CdSeTe was performed using a compound CdTe effusion source and an elemental Se effusion source. The alloy composition (x) of the $CdSe_xTe_{1-x}$ ternary compound was controlled through the Se:CdTe flux ratios. Our results indicated that the crystalline quality of CdSeTe decreases as the alloy composition increases, possibly due to an alloy disordering effect. A similar trend was observed for the CdZnTe ternary alloy system. However, the alloy disordering effect in CdSeTe was found to be less severe than that in CdZnTe. We have carried out the growth of CdSeTe on Si at different temperatures. An optimized growth window was established for CdSeTe on Si(211) to achieve high crystalline quality CdSeTe/Si layers with 4% Se. The as-grown layers exhibited excellent surface morphology, low surface defect density (less than 500 cm^{-2}), and low x-ray full width at half maximum (FWHM) values near 100 arcsec. Additionally, CdSeTe/Si layer exhibited excellent lateral uniformity.

15. SUBJECT TERMS

CdSeTe, Si, HgCdTe, CdTe, MBE, LWIR, defects, IR, II-VI

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Contents

List of Figures

1. Introduction

Successful direct growth of CdTe on Si(001) by molecular beam Epitaxy (MBE) was first demonstrated in 1989 (*1*), which stimulated strong interest in the HgCdTe community to develop techniques to grow high quality CdTe/Si layer as an alternative substrate for HgCdTe. For over a decade, the HgCdTe research community has made a considerable effort to establish MBE growth of CdTe/Si composite substrates for HgCdTe material growth and infrared device applications (*2–7*). This research has led to the development of a relatively mature MBE growth process for high quality CdTe/Si. Currently, CdTe/Si substrates are being used to grow HgCdTe to fabricate large-format short wavelength infrared (SWIR) and medium wavelength infrared (MWIR) HgCdTe infrared focal plane arrays (*8, 9*). Despite the tremendous advancements made in CdTe/Si material quality over the years, fabrication of long-wave infrared (LWIR) devices made from HgCdTe grown on CdTe/Si composite substrates has not been as successful due to the relatively high dislocation density on HgCdTe caused by the lattice mismatch between CdTe/Si and HgCdTe. To mitigate the lattice mismatch issue, initial effort was focused on incorporating 4.3% Zn into the CdTe/Si layer. However, we observed that CdZnTe/Si layers with lower defects and suitable crystal quality are difficult to achieve. Furthermore, it has been shown that the degradation of crystalline structure of $Cd_{1-y}Zn_yTe$ occurs for increasing Zn composition due to a miscibility gap (*10*). Therefore, it is very desirable to develop a novel ternary system that is lattice-matched to LWIR HgCdTe. In this work, we investigated an alternative material system, $CdSe_xTe_{1-x}$/Si, as a lattice matched composite substrate for LWIR HgCdTe. Growth of CdSeTe/Si, which occurs through anion mixing, will also be a good comparison to the growth of CdZnTe/Si, which occurs through cation mixing. In addition to its possible application as a composite substrate for LWIR HgCdTe, CdSeTe has the potential use for x-ray and gamma-ray detectors (*11*).

2. Experimental

2.1 Substrate Preparation

The substrates used for the growth are 3-in Si(211) wafers. The Si wafers were either lightly phosphor-doped or undoped with resistivity in the range of 10–50 ohm-cm. It is important to keep the resistivity above 10 ohm-cm to ensure that the infrared (IR) transmission is above 70% in the 1–12 micron spectrum range. The P-type Si wafer tends to have higher IR absorption. Before being introduced into the vacuum chamber, Si wafers were cleaned using a modified

process based on conventional RCA process (*12*). The process is illustrated in the following order:

1. Prepare five glass beakers and one plastic beaker with 1000 ml capacity. Fill the plastic beaker with 950 ml of de-ionized water (DIW) and 50 ml hydrogen fluride (HF) (49%) to make a diluted HF solution. Etch each glass beaker with the dilute HF solution and then rinsing with DIW. The clean beakers were filled with DIW and set aside for later use.
2. Fill one glass beaker with 600 ml DIW, 120 ml ammonium hydroxide (NH_4OH), and 120 ml hydrogen peroxide ($H_2O_{2)}$ (referred to as NH_4OH solution), and place the beaker on a hot plate.
3. Place the 3-in Si wafer onto a talon wafer holder. Blow the wafer surface with dry nitrogen gas to remove any dust particles attached to the surface. Insert the wafer into NH_4OH solution and heat for 30 min.
4. Use the plastic beaker to make a fresh diluted HF solution, as described in step 1.
5. Fill another glass beaker with 600 ml DIW and 120 ml hydrogen chloride (HCl) (37%) (referred to as HCl solution), and place the beaker on a hot plate.
6. Bring the beaker with NH_4OH solution together with the Si wafer remaining submerged and place under running DIW until the liquid is near room temperature.
7. Fill the remaining three glass beakers with fresh DIW. Rinse the Si wafer in fresh DIW for seven consecutive bathes.
8. Add 120 ml H_2O_2 into heated HCl solution.
9. Remove Si wafer from DIW and submerge into prepared HF solution and etch for 100 s to strip native oxide from Si surface.
10. At the end of etching slowly remove the Si wafer from HF solution (wafer will remain complete dry) and submerge the wafer into heated HCl solution and heated for 10 min.
11. Bring down the beaker with HCl solution together with Si wafer remaining submerged and place under running DIW until the liquid is at about room temperature.
12. Repeat step 7 to rinse the Si wafer in fresh DIW for 7 consecutive bathes.
13. Place Si wafer on a spinner and spin dry at 3000 rpm.
14. Place the dry Si wafer onto an indium-free substrate holder and load into vacuum chamber

2.2 Growth Process

Growth of $CdSe_xTe_{1-x}$ on Si was conducted using a DCA MBE system equipped with a 3.25-in substrate heater. Three-inch Si(211) nominal wafers were used as substrates. All Si wafers were cleaned using the modified RCA process, as described in section 2.1. This process leaves an approximate 12 Å uniform oxide layer on the Si surface, which must be thermally removed in the growth chamber. For these experiments, the samples were quickly heated to 1050 °C to remove the oxide layer and then quickly cooled under an As_4 flux to 500 °C. Finally, the sample was cooled to the nucleation temperature of 340 °C without any flux. Note that all temperatures stated are the reading of a thermocouple, which is located approximately 10 mm from the back of the substrate. Although the thermocouple does not measure the precise temperature of the sample surface, this configuration provides both excellent temperature control and run-to-run reproducibility.

The growth of CdSeTe starts with a seeding layer of thin ZnTe deposited at 340 °C on Si substrate, using migration-enhanced epitaxy (MEE) (*5*) with elemental Zn and Te sources. After annealing the ZnTe layer at 490 °C with Te flux for 20 min, we grew a thick (~6 micron) CdTe layer using a CdTe compound source. The growth rate of CdTe is approximately 0.65 µm/h. Periodically, during CdTe growth, the layer was briefly annealed to 530 °C under a Te over pressure. This type of flash annealing was used to improve the CdTe layer quality. Finally, $CdSe_xTe_{1-x}$ was grown on top of the CdTe layer using the CdTe compound source and an elemental Se source. The temperature profile of the baseline growth process is illustrated in figure 1. For these experiments, no annealing sequences were used during CdSeTe growth. CdTe and CdSeTe growth temperatures were identical and were varied between 320 °C and 440 °C for this study. The baseline growth parameters, such as CdTe and CdSeTe growth temperatures, Se and CdTe fluxes were optimized against CdSeTe surface morphologies, crystalline quality, alloy composition, and structural defect density.

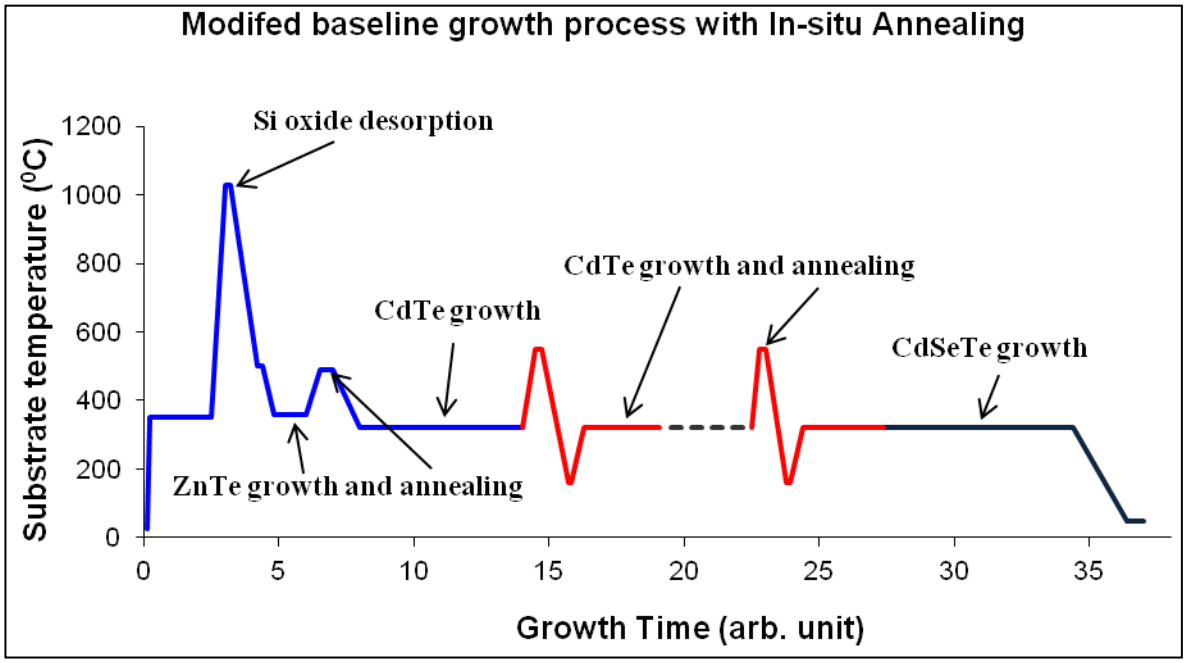

Figure 1. Temperature profile of baseline MBE growth process of CdSeTe on Si(211).

2.3 Material Characterization

As-grown $CdSe_xTe_{1-x}$ layers were evaluated with x-ray rocking curve measurements in order to gauge the overall crystalline quality. Additionally, we used x-ray diffraction to calculate the composition of the CdSeTe layer by determining the offset of the CdSeTe peak with respect to the position of the CdTe peak, and assuming a linear relationship between alloy composition and $CdSe_xTe_{1-x}$ lattice constant. Such a linear relationship has been confirmed for $CdSe_xTe_{1-x}$ polycrystalline films deposited on glass using electron beam evaporation (*13*). Based on these assumptions, we calculated that 4.0% Se incorporation is needed in CdTe to achieve lattice matching with LWIR $Hg_{0.78}Cd_{0.22}Te$.

Surface morphologies of CdSeTe/Si layers were examined by an optical microscope equipped with a digital camera.

Thicknesses of the CdSeTe/Si layers were estimated from interference fringes of IR transmission spectra, as shown in figure 2. Considering light passing through a thin film, the thickness (t) of the thin film can be expressed as a function of the interference fringe separation (Δ):

t (cm) = $1/(2n\Delta)$, where n is the refraction index of the thin film

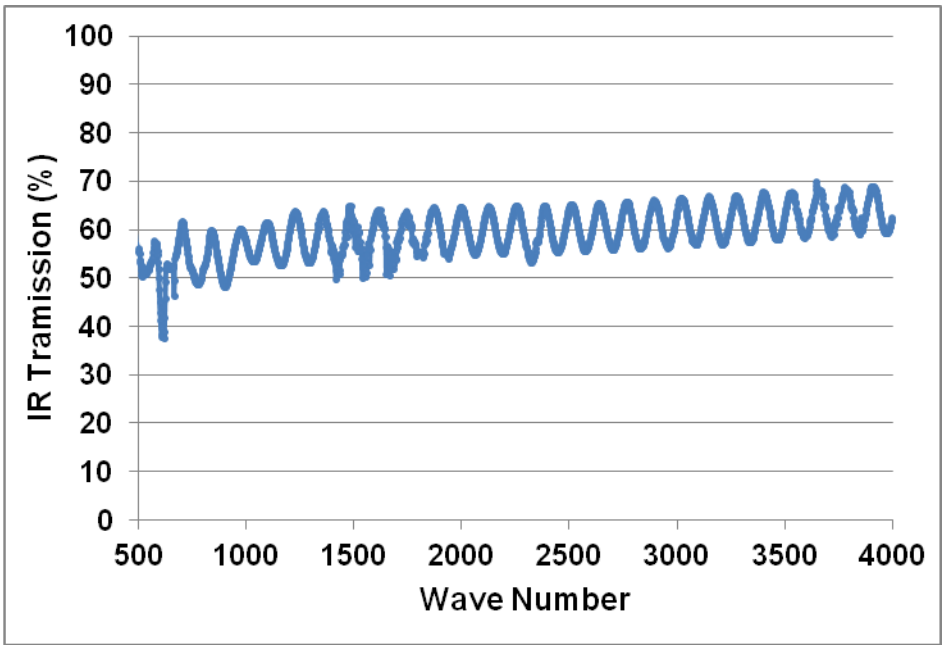

Figure 2. IR transmission spectrum of a CdSeTe grown on Si(211).

To properly control the Se concentration, careful flux measurements of the Se source and the CdTe source were made prior to each MBE growth run using a retractable ion gauge placed in the sample growth position.

3. Results and Discussion

3.1 Control of Alloy Composition

In order to study material characteristics with respect to Se composition, we have grown CdSeTe layers with different alloy compositions, which was achieved through control of the Se:CdTe beam equivalent pressure (BEP) ratios. During CdSeTe growth, Se and Te are in competition for the same nucleation sites. If we assume that all Cd atoms impinging on the substrate are incorporated, the maximum number of Se and Te atoms incorporated should be equal to the number of Cd atoms, which is proportional to the Cd flux. Since we are using a single CdTe cell to provide Cd and Te flux, we expect equal numbers of Cd and Te atoms due to congruent evaporation of the II-VI compound. Furthermore, if we assume total incorporation of incoming Se atoms into the CdSeTe layer, the alloy composition of the ternary compound can be calculated as $x(cal) = \Phi_{Se}/(\Phi_{Se} + \Phi_{Te})_{incorporated}$. Since $(\Phi_{Se} + \Phi_{Te})_{incorporated} = \Phi_{Cd} = \Phi_{CdTe}/2$, therefore, $x(cal) = \Phi_{Se}/\Phi_{Cd} = 2\Phi_{Se}/\Phi_{CdTe}$, where Φ is the BEP of the material, measured by the nude ion gauge at the substrate position. Figure 3 shows the relationship between the calculated

Se composition, based on Se:CdTe BEP ratio, and the measured alloy composition determined by x-ray diffraction. The results indicated that the measured values were always smaller than the calculated values, which implies that not all the Se atoms impinging on the substrate were incorporated into the CdTe matrix due to a competition between Te and Se atoms. Furthermore, the deviation increases as the alloy composition increases. The measured alloy composition seems to saturate at approximately 60% when the alloy was grown using only CdTe + Se fluxes, even under Se rich conditions. Using this empirical relationship, one can effectively control the alloy composition of CdSeTe by varying the Se:CdTe BEP ratio.

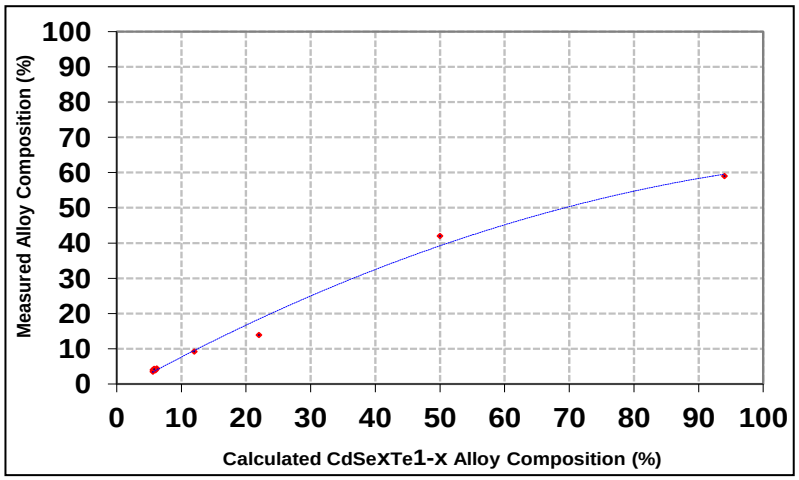

Figure 3. Relationship between calculated alloy compositions based on Se/CdTe BEP ratio and measured alloy compositions. The dash line is the guiding trend line and the solid line is the equilibrium line

3.2 Alloy Disordering Effects in the CdSeTe Ternary System

In order to study the alloy disordering effects in the CdSeTe ternary system, we performed x-ray rocking curves measurement on many CdSeTe/Si layers with different alloy compositions. Figure 4 illustrates the relationship between the x-ray full width at half-maximum (FWHM) of CdSeTe/Si layers and the alloy composition. Broadening of the x-ray FWHM of the ternary alloy is usually related to the alloy disordering. Our past studies on CdZnTe/Si indicated that the broadening of the x-ray FWHM of CdZnTe/Si varies from 70–360 arcsec as the Zn concentration increases from 0 to 10%. In comparison, the x-ray FWHM of the CdSeTe layers varies from 70–230 arcsec as the Se concentration increases from 0 to 10%, respectively. From this measurement, it appears that the alloy disordering is less prevalent in the CdSeTe alloy than in the CdZnTe alloy, which is certainly encouraging for the development of CdSeTe/Si as a composite substrate for HgCdTe. Furthermore, as shown in the inset in figure 4, broadening of

the x-ray FWHM does not substantially occur until the composition reaches 4%. Since only 4% Se is needed to lattice-match CdSeTe to LWIR HgCdTe, alloy disorder may be a negligible effect in producing alternative substrates.

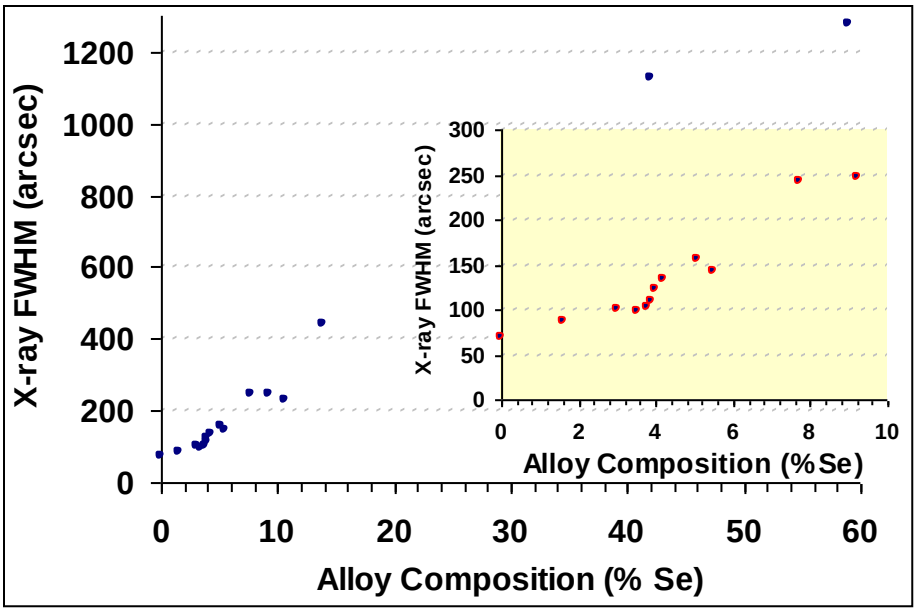

Figure 4. X-ray FWHMs of CdSeTe/Si layers as a function of alloy composition.

3.3 Growth Optimization

Since there have been no previous studies on the growth of CdSeTe on Si by MBE, we experimented with a wide variety of parameters in order to optimize growth conditions, one of which is the growth temperature. We have grown CdSeTe/Si with 4.0 ± 0.2% Se, using CdTe + Se fluxes under different growth temperatures. The quality of the layers was evaluated by their x-ray FWHM, surface morphology, and surface defect density. In our investigation, the growth temperature of CdSeTe on CdTe/ZnTe/Si was varied from 320–440 °C. Figure 5 shows the x-ray FWHMs of CdSeTe layers as a function of the CdSeTe growth temperatures. A trend of slightly increasing x-ray FWHM values is observed as the growth temperature increases. Similar trends were also observed for surface defects and surface morphologies as a function of CdSeTe growth temperature, as is shown in figures 6 and 7. The surface morphology of CdSeTe becomes significantly rougher as the growth temperature increases. Our results indicate that the growth of better CdSeTe layers, as determined by the surface morphology, can be achieved in a growth window of 320–420 °C, which is larger than we expected. However, considering all these criteria, such as surface morphology, defect density and x-ray FWHM, we determined that the optimized growth window for the best CdSeTe/Si layers with 4.0 ± 0.2% Se is 340–380 °C.

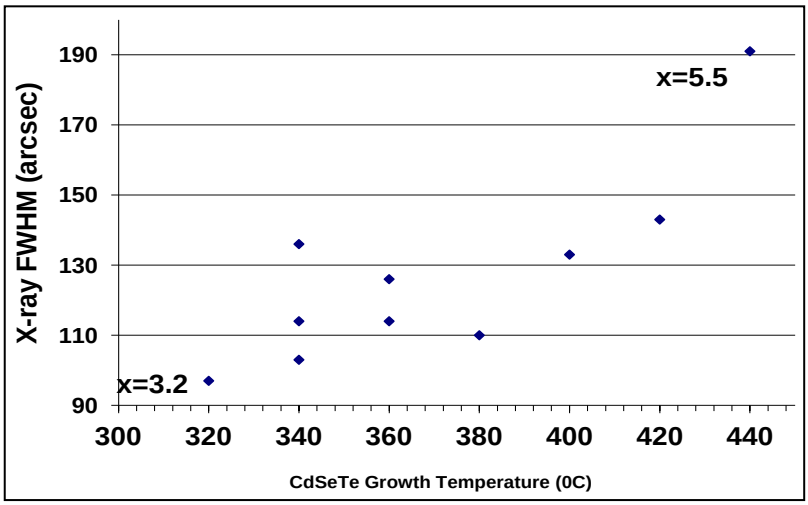

Figure 5. X-ray FWHMs of CdSeTe layers with Se composition of 4.0 ± 0.2% vs CdSeTe growth temperature.

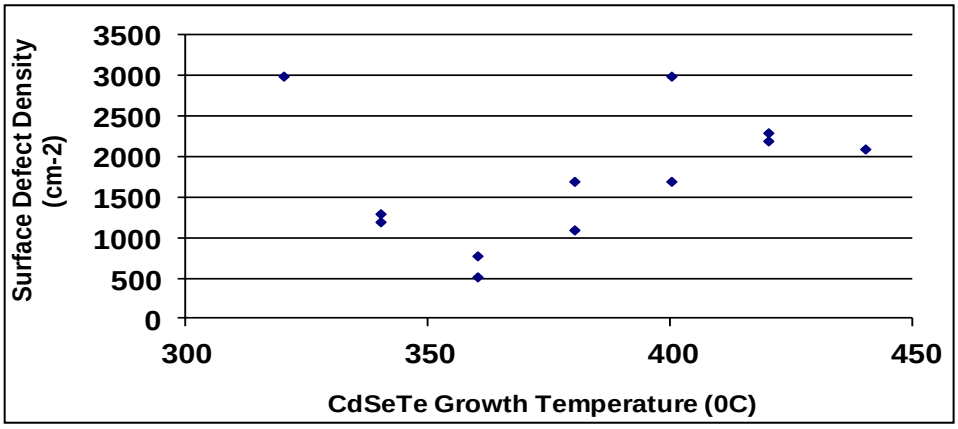

Figure 6. Surface defect density of as-grown CdSeTe/Si with Se composition of 4.0 ± 0.2% as a function of CdSeTe growth temperature.

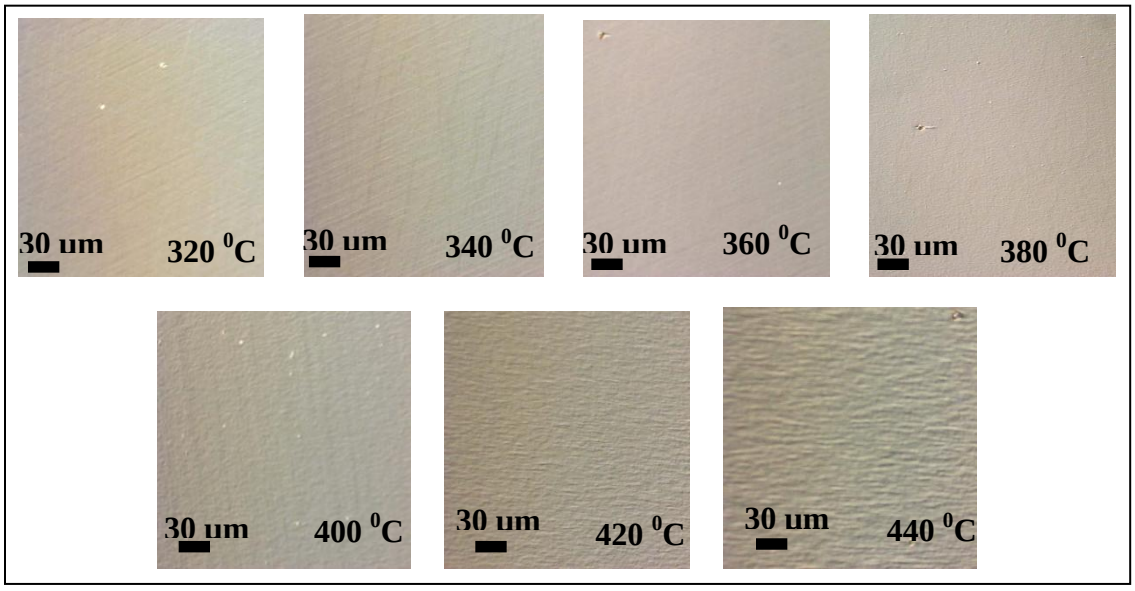

Figure 7. Surface morphologies of as-grown CdSeTe/Si layers with Se composition of 4.0 ± 0.2% grown at different temperatures

One of the primary motivations to develop CdTe/Si composite substrates is to provide low cost, large size substrates for large-format HgCdTe focal plane arrays (FPAs). One of the key parameters for the large-format FPAs is the lateral uniformity of the detector material properties. For this reason, we performed a uniformity test of a 3-in $CdSe_{0.04}Te_{0.96}$/Si(211) wafer. Figure 8 shows lines scans across the 3-in wafer for layer thickness, alloy composition, and x-ray FWHM. The scans were performed manually through a point-by-point measurement. Since the 3-in CdSeTe wafer was grown with substrate rotation throughout the growth process, 2-D lateral uniformity can be effectively represented by the radial uniformity. The results indicate that 3-in CdSeTe/Si wafers grown by MBE exhibit excellent lateral uniformity, which is a necessary feature of a composite substrate, used for large format LWIR HgCdTe FPAs.

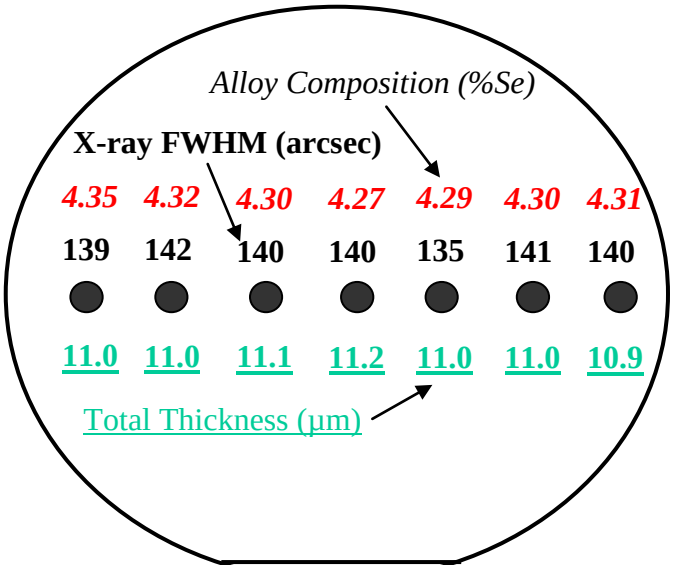

Figure 8. Point-by-point lateral measurement of film thickness, x-ray FWHM and alloy composition of a 3-inch CdSeTe/Si wafer.

4. Conclusions

We have established a baseline MBE growth process to produce high quality Si base composite substrate, CdSeTe/Si lattice matched to LWIR HgCdTe. The growth of CdSeTe was achieved using a CdTe compound source and an elemental Se source. Alloy composition can be controlled by the Se:CdTe BEP ratios. X-ray FWHM of $CdSe_xTe_{1-x}$/Si increases as the alloy composition increases. However, CdSeTe/Si with 4% Se incorporated exhibits excellent surface morphology, low surface defect density (< 500 cm^{-2}), excellent lateral uniformity, and an x-ray FWHM of 101 arcsec. These values represent the best LWIR lattice matching composite substrate layer properties. Our results demonstrated that $CdSe_{0.04}Te_{0.96}$/Si(211) composite substrate is a promising lattice matching substrate for large format LWIR HgCdTe FPAs.

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List of Symbol, Abbreviation, and Acronyms

BEP	beam equivalent pressure
DIW	de-ionized water
FPAs	focal plane arrays
FWHM	full width at half-maximum
HCl	hydrogen chloride
HF	hydrogen fluride
H_2O_2	hydrogen peroxide
IR	infrared
LWIR	long wavelength infrared
MBE	molecular beam epitaxy
MEE	migration-enhanced epitaxy
MWIR	medium wavelength infrared
NH_4OH	ammonium hydroxide
SWIR	short wavelength infrared

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